This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims

1. (Currently Amended) A CMOS inverter comprising:

a heterostructure including a Si substrate, a SiGe graded buffer layer on the Si substrate, a relaxed $Si_{1-x}Ge_x$ layer on ~~said Si substrate~~the SiGe graded buffer layer, and a strained ~~surface~~ channel layer on ~~said~~ the relaxed $Si_{1-x}Ge_x$ layer, the heterostructure further including a smoothed surface positioned between the strained ~~surface~~ channel layer and the Si substrate, ~~the surface and~~ the strained channel layer having an average roughness less than 1 nm; and

a pMOSFET and an nMOSFET, wherein the channel of said pMOSFET and the channel of said nMOSFET are formed in said strained ~~surface~~ channel layer.

2. (Cancelled)

3. (Cancelled)

4. (Cancelled).

5. (Cancelled).

6. (Original) The CMOS inverter of claim 1, wherein the strained ~~surface~~ channel layer comprises Si.

7. (Original) The CMOS inverter of claim 1, wherein $0.1<x<0.5$.

8. (Original) The CMOS inverter of claim 7, wherein the ratio of gate width of the pMOSFET to the gate width of the nMOSFET is approximately equal to the ratio of the electron mobility and the hole mobility in bulk silicon.

9. (Original) The CMOS inverter of claim 7, wherein the ratio of gate width of the pMOSFET to the gate width of the nMOSFET is approximately equal to the ratio of the electron mobility and the hole mobility in the strained ~~surface~~ channel layer.

10. (Original) The CMOS inverter of claim 7, wherein the ratio of gate width of the pMOSFET to the gate width of the nMOSFET is approximately equal to the square root of the ratio of the electron mobility and the hole mobility in bulk silicon.

11. (Original) The CMOS inverter of claim 7, wherein the ratio of gate width of the pMOSFET to the gate width of the nMOSFET is approximately equal to the square root of the ratio of the electron mobility and the hole mobility in the strained ~~surface~~ channel layer.

12. (Original) The CMOS inverter of claim 7, wherein the gate drive is reduced to lower power consumption.

13. (Cancelled).

14. (Cancelled).

15. (Currently Amended) An integrated circuit comprising:

a heterostructure including a Si substrate, a SiGe graded buffer layer on the Si substrate, a relaxed $Si_{1-x}Ge_x$ layer on ~~said Si substrate,~~the SiGe graded buffer layer, and a strained ~~surface~~ channel layer on ~~said~~ the relaxed $Si_{1-x}Ge_x$ layer, the heterostructure further including a smoothed surface positioned between the strained ~~surface~~ channel layer and the Si substrate, ~~the surface and~~ the strained channel layer having an average roughness less than 1 nm; and

a p-channel transistor and an n-channel transistor formed in said heterostructure, wherein said strained channel layer comprises the channel of said n-channel transistor and said p-channel transistor, and said n-channel transistor and said p-channel transistor are interconnected in a CMOS circuit.

16. (Cancelled).

17. (Cancelled)

18. (Cancelled).

19. (Cancelled).

20. (Original) The integrated circuit of claim 15, wherein the strained layer comprises Si.

21. (Original) The integrated circuit of claim 15, wherein $0.1<x<0.5$.

22. (Original) The integrated circuit of claim 15, wherein the CMOS circuit comprises a logic gate.

23. (Original) The integrated circuit of claim 15, wherein the CMOS circuit comprises a NOR gate.

24. (Original) The integrated circuit of claim 15, wherein the CMOS circuit comprises an XOR gate.

25. (Original) The integrated circuit of claim 15, wherein the CMOS circuit comprises a NAND gate.

26. (Original) The integrated circuit of claim 15, wherein the p-channel transistor serves as a pull-up transistor in said CMOS circuit and the n-channel transistor serves as a pull-down transistor in said CMOS circuit.

27. (Original) The integrated circuit of claim 15, wherein the CMOS circuit comprises an inverter.